CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A method of forming a raised source/drain field effect transistor including the steps of:

etching a gate region sufficient for silicidation of contacts in a substrate;

forming a gate structure at said gate region;

growing boron doped amorphous silicon on NFET and PFET regions, adjacent said gate region, by selective epitaxy;

forming an abrupt source/drain junction for PFET boron extension electrode and NFET boron halo formation adjacent said gate region; and

etching dual spacers in said source/drain junction.

2. The method of claim 2, further comprising the steps of:

performing N-extension arsenic implantation and P-extension boron implantation; and

diffusing said arsenic and said boron such that said PFET extension electrode overlaps the gate region.

3. The method of claim 2, where the N-extension arsenic does not substantially overlap the gate region.

4. The method of claim 1, further comprising the step of performing selective amorphous growth to form the source/drain junction.

5. A CMOS Structure comprising:

a gate region of a substrate sufficient for silicidation of contacts;

a gate structure at said gate region;

a PFET boron extension electrode and NFET boron halo, defining a source/drain junction, adjacent said gate region; and

permanent dual spacers in said source/drain junction.

6. The CMOS Structure of claim 5, where the PFET extension overlaps the gate region.

7. The CMOS Structure of claim 6, where the N-extension arsenic does not substantially overlap the gate region.